White paper

endura technologies

Fast Switching Power Delivery Architecture for DDR5 and Computing Applications

Introduction

DDR5 is a substantial advancement over DDR4 and requires power management solutions that support the new memory standard.

While DDR5 reduces memory voltage to 1.1V (vs 1.2V), maximum memory density is increased by 8x and overall speeds by 2x which significantly effects power requirements as discussed below.

"In August 2021, Samsung revealed a 512 GB 7200 MHz RAM DIMM.[2] While previous SDRAM generations allowed unbuffered DIMMs that consisted of memory chips and passive wiring (plus a small serial presence detect ROM), DDR5 DIMMs require additional active circuitry, making the interface to the DIMM different from the interface to the RAM chips themselves.

DDR5 (L)RDIMMs use 12 V and UDIMMs use 5 V input. DDR5 DIMMs are supplied with management interface power at 3.3 V, [19][20] and use on-board circuitry (a power management integrated circuit [21] and associated passive components) to convert to the lower voltage required by the memory chips. Final voltage regulation close to the point of use provides more stable power and mirrors the development of voltage regulator modules for CPU power supplies." (Wikipedia, 2022)

With the above, Samsung also introduced 3 new PMICs to support their DDR5 products for Data Center, Server, and PC markets. (Samsung, 2021)

For DDR5 and other computer applications like Solid State Drives (SSD), Endura Technologies has partnered with leading memory companies and developed a JEDEC-compliant solution leveraging its fast-switching power delivery architecture. With these solutions, designs can operate at JEDEC specs or switch at higher speeds based on their system needs.

This power delivery architecture allows a system to be tailored to the application with the following benefits:

- flexibility to operate across a broader range of switching frequencies
- higher efficiencies by matching the switching speed to the current load profile and range
- optimized component count and footprint
- digital load monitoring for artifact-free leg and phase shedding
- load-aware DVFS to adjust frequency and voltage within the system

Fast Switching Power Delivery Architecture

Previous generations of Power Management Integrated Circuits (PMICs) were based on the DC-DC Converter. To meet modern demands, the DC-DC converter must achieve near-perfect efficiency; change regulated voltage instantaneously; maintain load regulation under stringent transients; and switch at higher speeds to reduce passive components form factors.

Historically PMICs have used older process nodes and associated Bipolar CMOS DMOS (BCD) variants. Foundries now provide high voltage capabilities on advanced process nodes allowing for faster switching speeds with minimal efficiency deltas, a key for new architectures.

Endura Technologies' new architecture, the Bypass Dual Duty Cycle Control (BDDC^{TM}), leverages this trend to provide new power delivery features:

- Unconditionally stable control for fast switching and Dynamic Voltage Control (DVC)
- Flat efficiency via seamless transitions from Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM).
- Stable operation at high switching frequencies with no reliance on current sensing or zero crossing comparator; maximum frequency is set by the process and switching losses.
- Fast digital load current monitoring which provides:
    - Digital Leg and Phase Shedding
    - Proprietary Load-Aware DVFS (LA-DVFS^{TM})

Bypass Dual Duty Cycle Control Technology (BDDC)

Per Figure 1, two independent Pulse Width Modulation (PWM) Generators produce duty cycles of PWM_{base} and PWM_{adj}.

Under light load conditions, only PWM_{base} is used to keep the device in DCM mode. When V_{OUT} drops below tolerance, a PWM pulse is generated to switch on the Power Stages and regulate the output. Otherwise, no current is sent to C_{OUT} until load needs increase.

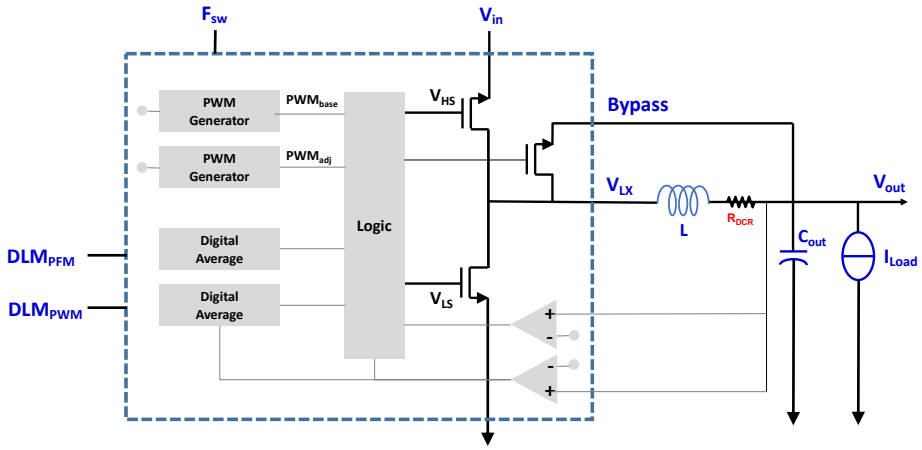


Figure 1: Simplified Bypass Dual Duty Cycle Control (BDDC) Architecture

In DCM, Pulse Frequency Modulation (PFM) is used. As the load increases, PFM becomes continuous, and the Output seamlessly transitions to CCM and PWM operation per Figure 2.

In CCM, the system oscillates between PWM_{base} and PWM_{adj} where PWM_{adj} is set to ensure proper regulation at maximum load.

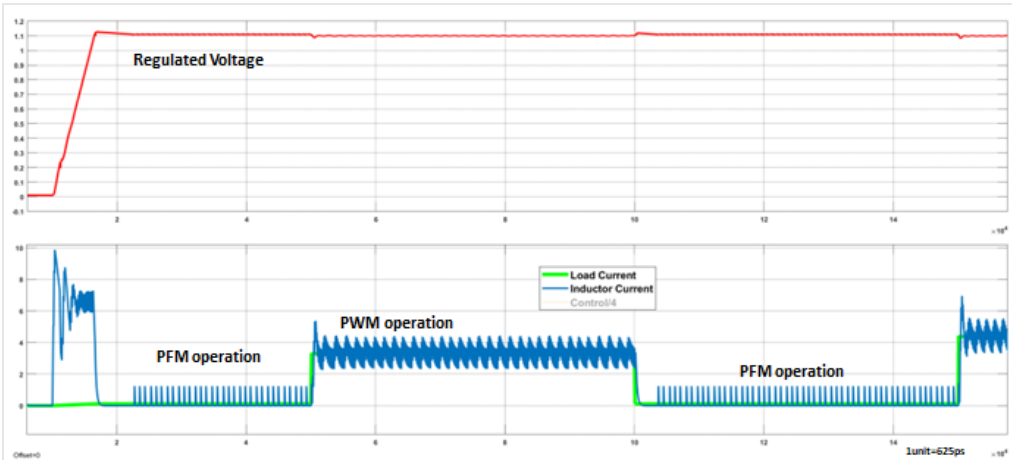


Figure 2: BDDC Start-up and Load Transient Regulation

Bypass Mode

Bypass Mode is only active in DCM and CCM overshoot conditions. With a CCM overshoot, the device automatically enters DCM and the internal Bypass Switch shorts inductor (L) which dissipates current in a free-wheeling loop. No additional current is sourced to the load.

This Bypass Switch also eliminates resonances which allows the system to operate at higher speed with unconditional stability. The benefits of Bypass Mode are:

- Eliminates ringing in DCM
- Prevents overshoot with high-to-low load transients
- Enables DVC ramping of V_{OUT} at the highest slew rate without ringing; see Figure 3

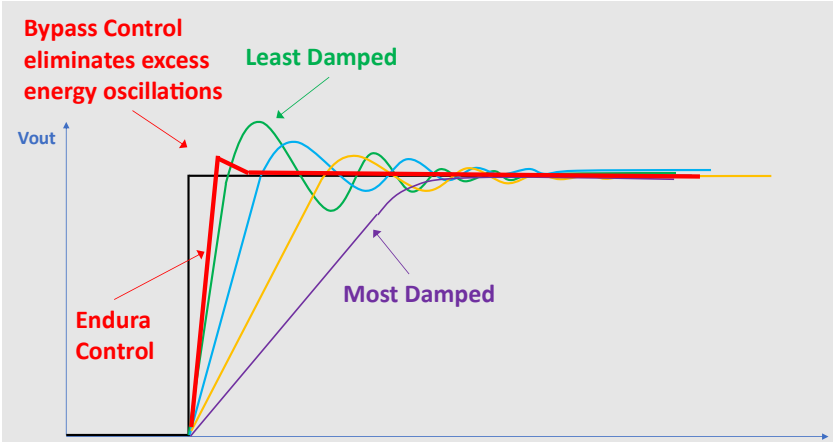
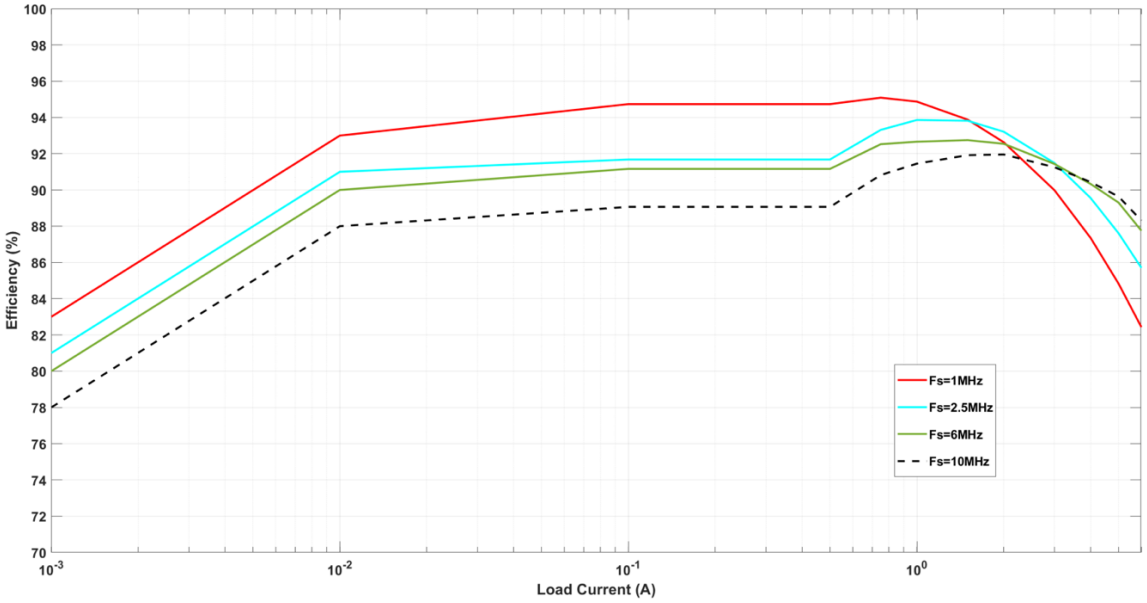


Figure 3: BDDC Bypass Mode Minimizes Ringing with Fast Slew Rates

Seamless PFM-PWM Transition

Per Figure 2, DCM (PFM mode) will automatically transition to CCM (PWM mode) as the load increases. When the load decreases to a set point, the Bypass Switch will engage and transition to DCM with PFM pulses regulating light load conditions. BDDC does not need current sensing or zero crossings which allows seamless PFM-PWM operation at the maximum switching speed.



Per Figure 4, efficiency is flat over a broad current load range during the PFM-PDM transitions.

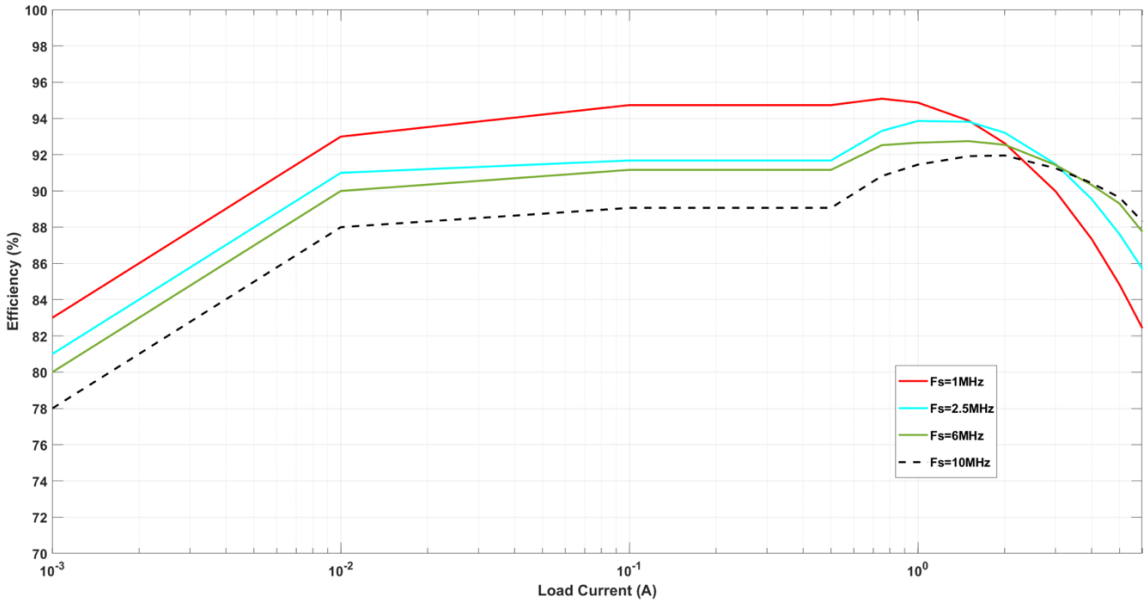


Figure 4: Estimated Efficiency over Load Current Range (Single-Phase, V_{IN} @ 3.6V, V_{OUT} @ 1.0V)

AC Regulation in Extreme Transients

To mitigate sub-harmonic ripple on V_{OUT}, a proprietary AC Regulation keeps ripple in the milli-volt range and does not affect stability. It protects against droop and overshoot with load transients.

Figure 5 shows a Single-Phase Buck regulated under varying load transient at a high slew rate with Seamless PFM-to-PWM operation maintained; ramps from 0 to 1.1V in 4uS.

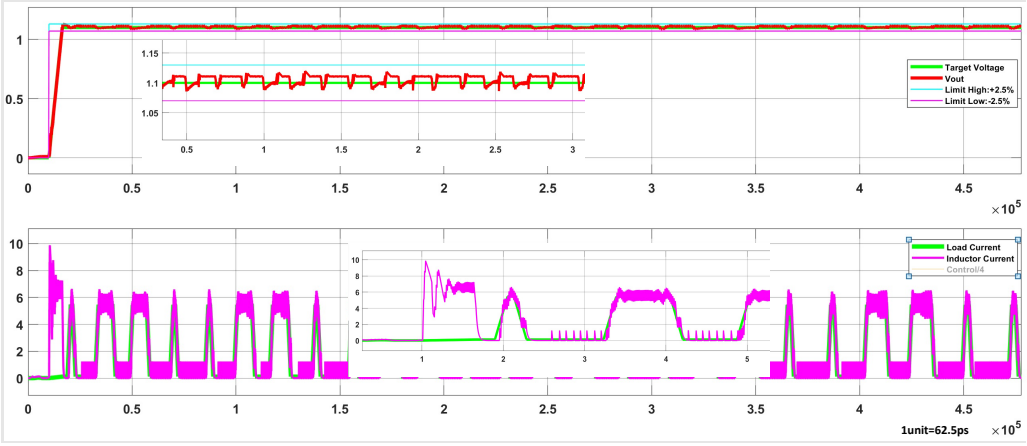


Figure 5: AC Regulation F_s = 10MHz, L=60nH, C_{OUT} = 20uF, Single Phase w/pseudo random transients at 7A/us

Digital Load Monitoring (DLM)

In CCM, the duty cycle between PWM_{adj} and PWM_{base} is linearly dependent on load current. Averaging the comparator bitstream provides an accurate digital signature of the load current as shown in Figure 6.

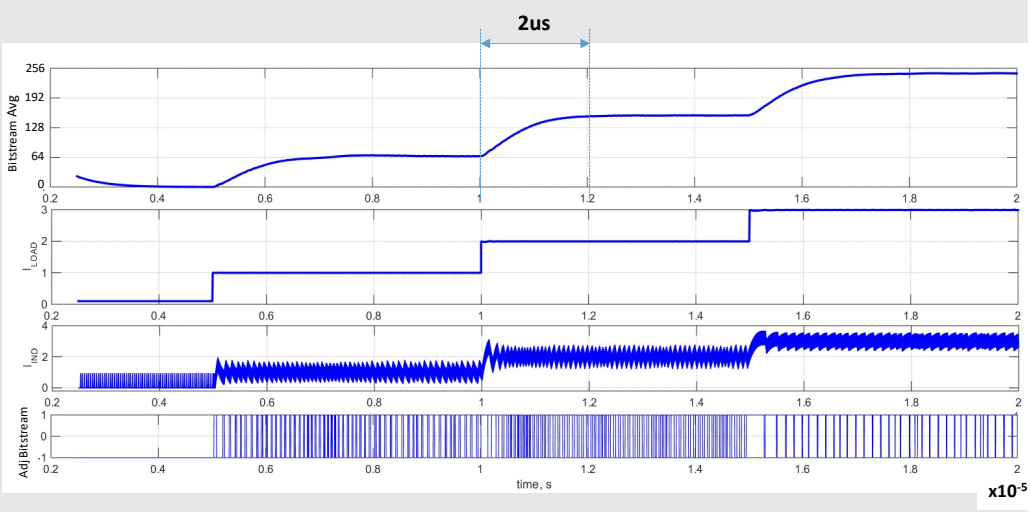


Figure 6: Fs = 20MHz, L=36nH, C_{OUT} = 10uF, Single Phase BDDC Reporting Current Steps in <2us

When not adjusting, the 8-bit comparator's average output is zero indicating light load. When adjusting, the comparator's average is 256 bits signaling the load is at the regulated maximum.

In DCM (PFM), the density of current pulses is proportional to the load current. Similarly, averaging the bypass comparator output provides the digital signature of the light load current.

DLM allows for effective Digital Leg and Phase Shedding in multi-phase operation. Used in combination with Endura Technologies' AC Regulation, it achieves artifact-free leg and phase shedding while increasing efficiency and extending load range.

Next, we discuss how rapid DLM can be used to significantly improve system efficiency with companion SoC's using Load-Aware Dynamic Voltage Frequency Scaling (LA-DVFS^{TM}).

Load-Aware DVFS Operation

Modern computer devices/systems consume energy as a function of applications which dynamically drive data transfer and computational demands. These varying loads must be addressed with low latency to improve performance and reduce energy consumption.

Dynamically adjusting digital clock frequencies and supply voltages is not new. The opportunity is reducing response latency so that energy is sourced only as needed; this translates into fast DVC.

With DLM providing the digital load signature in real time, the system is also made "load aware" in real time. This speed's up the ability to adjust frequency and voltage within the system with hardware and/or software.

Part of the solution is that BDDC can operate DC-DC converters at higher switching speeds. Endura has demonstrated multi-phase embedded voltage regulator (eVR^{TM}) at 150MHz (1V supply). We have also demonstrated a 5V DC-DC converter at 20MHz with DLM of <2us latency. This enables micro-second (potentially less) hardware-based LA-DVFS while also enabling extremely fast software-based LA-DVFS.

DCDC Loss Breakdown

Per Figure 7, DCDC converters incur capacitive and resistive losses. Capacitive losses increase proportionally at higher frequencies and materialize in charging and discharging power MOSFET capacitances. Resistive losses are constant and consist of losses of MOSFET R_{DSON}, DCR of inductors, and PCB parasitic resistances of the traces.

The Endura Technologies DLM-enabled Automatic Leg Shedding algorithm makes R_{DSON} resistive losses non-dominant at heavy loads. Inductor DCR and trace parasitic resistance becomes loss-dominant at heavy load.

Inductor sizes reduce as a square root of the speed increase factor and the output capacitors reduce proportionally. The smaller inductor leads to a smaller DCR, and a smaller PCB footprint leads to smaller metal trace parasitic resistances, $R_{PX,}$ and R_{PO} as depicted in Figure 7.

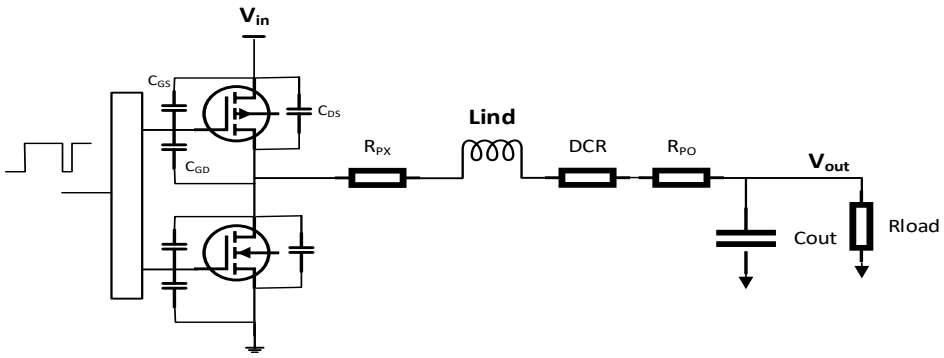


Figure 7: Illustration of Capacitive (switching) and resistive losses in a DCDC converter

Efficiency Improvement

Reductions in DCR and PCB trace resistances improve efficiencies at heavier loads. Figure 8 illustrates efficiencies for switching frequencies across a load range. Depending on the application, a design can choose a switching frequency to optimize overall efficiency.

For example, 1 MHz switching would be ideal for applications with <1A needs. Whereas applications with >2A needs, would benefit by switching faster. The key is switching frequency is tailorable to the application to optimize efficiency.

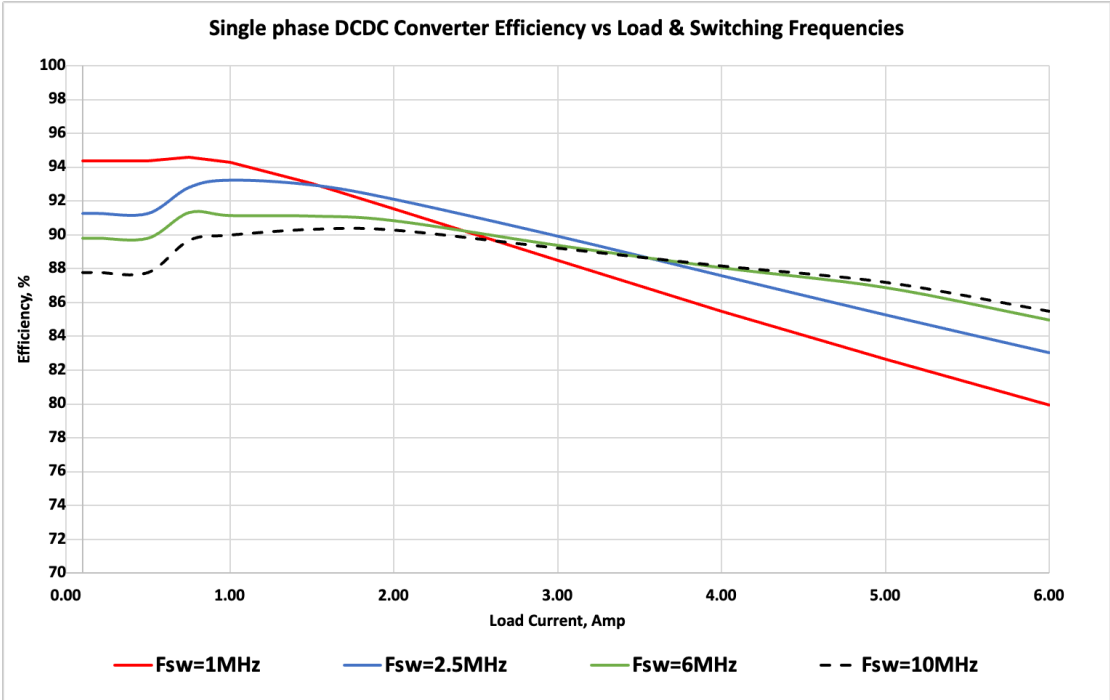


Figure 8: Estimated Efficiency versus Load Current at different Switching Frequencies

Component and Footprint Reduction

Higher switching speed enables a substantial reduction in the system components and footprint.

Table 1 describes the passive component count and estimated areas for a variety of switching frequencies. This illustrates the advantage of higher switching speeds and provides flexibility for systems when area and/or costs are a primary concern.

Switching Frequency	Local Passives	Distributed Passives	Total Passive Values	Total Passives	Passive Size X mm	Passive Size Y mm	Passive Area mm^2
1MHz	680nH	na	Total	1	3.20	2.50	20.8
	47uF x2	47uF x8	470uF	10	1.60	0.80	
2.5MHz	220nH	na	220nH	1	2.50	2.00	10.12
	47uF	47uF x3	188uF	4	1.60	0.80	
6MHz	100nH	na	100nH	1	2.00	1.20	4.96
	22uF	47uF	69uF	2	1.60	0.80	
10MHz	60nH	na	60nH	1	1.00	0.50	3.06
	22uF	22uF	44uF	2	1.60	0.80	

Table 1: Required Components and Area by Switching Frequency

BDDC and Constant On-Time (COT) Architectures

While COT is proven for high voltage applications, the architecture relies on current sensing and zero-crossing comparators; as the switching frequency increases so does the power due to higher quiescent current. Above 3MHz, current sensing becomes erratic, and the zero-crossing comparator needs to detect many microvolts in a brief period which requires a substantial amount of quiescent current. At 10MHz it is nearly impossible for COT to keep regulation.

The BDDC architecture is not limited by switching frequency. As outlined in Table 2, at lower switching frequencies, it is comparable with COT. As the frequency increases, BDDC provides better regulation and performance.

Architecture	Switching Frequency Regulation		
	1 MHz	3 MHz	10 MHz
COT	Excellent	Higher Quiescent Current	Difficult to Regulate
BDDC	Excellent	Very Good	Lower at Light Load Better at Heavy Load

Table 2: BDDC & COT at Switching Frequency Regulation

Table 3 describes the load transient regulation of each architecture.

Architecture	Load Transient Regulation		
	Undershoot Response	Overshoot Response	Peak-to-Peak
COT	Immediate	Slower; needs to dissipate Inductor current	Poor
BDDC	Medium, 1/2 CLK period	Immediate	Excellent

Table 3: BDDC & COT at Load Transient Regulation

JEDEC Compliance

The solution is an integrated power delivery solution for DDR5 SODIMM and UDIMM applications and fully compliant to the JEDEC PMIC5100.

Per Figure 1, the input power supply (V_{IN}) is regulated for all DIMM components and consists of three step-down switching output regulators (SWA, SWB, SWC), two LDO output regulators plus I2C/I3C interface with embedded Multi-Time Programmable (MTP) NVM.

The solution is pin-to-pin compatible with JEDEC PMIC5100 devices.

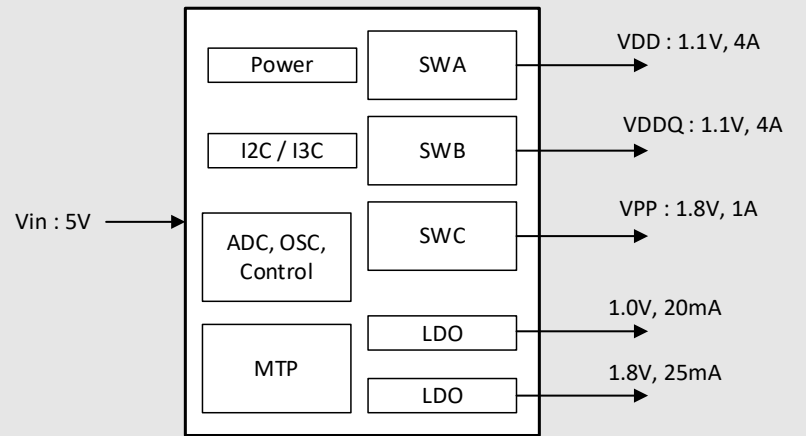


Figure 9: Power Conversion Block Diagram

Feature List

- Single V_{IN} from 4.25V to 5.5V
- Three DC-DC Buck Converters: SWA, SWB, SWC; Dual-phase configurability for SWA, SWB
- Two LDOs: V_{OUT}_1.0V, V_{OUT}_1.8V
- Output Voltage rail protection: OVP, UVP, OCP on all DC-DC output rails
- Input Voltage protection: UVP, OVP on VIN rail
- Thermal protection: Temperature warning and critical temperature shutdown
- Independently programmable output voltages and power sequencing for DC-DC converters
- Output current and power measurement, output current threshold mechanism
- Power Good status indicator
- General Status Interrupt function (GSI)
- Flexible Open Drain IO (I2C) and Push Pull (I3C Basic) IO Support
- Flexible Enable for DC-DC by VR_EN pin or VR Enable command
- Multi-time programmable non-volatile memory with secured R/W access
- Persistent error log registers
- Secure and programmable operation modes
- Error injection capability supported
- Programmable and DIMM specific registers for customization
- Idle power state

JEDEC Compliant Electrical Spec

Parameter	Symbol	Min	Typ	Max	Unit
Output Voltage	V_{OUT}		1.1		V
Maximum Continuous DC Load Current	I_{tdc}	0	-	4	A
Maximum Peak Instantaneous Current	$I_{peakmax}$	-	-	5	A
Maximum Load Transient	dI/dt	-	-	7	A/µs
Regulator Output DC+AC Voltage Tolerance	Reg_DC_AC_Tol	-2.5		2.5	%
Regulator Feedback Setpoint Accuracy	FB_Set_Point	-0.75		0.75	%

Table 4: SWA, SWB Single Phase Regulator; DC+AC Specification

Parameter	Symbol	Min	Typ	Max	Unit
Output Voltage	V_{OUT}		1.1		V
Maximum Continuous DC Load Current	I_{tdc}	0	-	8	A
Maximum Peak Instantaneous Current	$I_{peakmax}$	-	-	10	A
Maximum Load Transient	dI/dt	-	-	14	A/µs
Regulator Output DC+AC Voltage Tolerance	Reg_DC_AC_Tol	-2.5		2.5	%
Regulator Feedback Setpoint Accuracy	FB_Set_Point	-0.75		0.75	%

Table 5: SWA + SWB Dual Phase Regulator, DC+AC Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Output Voltage	V_{OUT}		1.8		V
Maximum Continuous DC Load Current	I_{tdc}	0	-	1	A
Maximum Peak Instantaneous Current	$I_{peakmax}$	-	-	2	A
Maximum Load Transient	dI/dt	-	-	2.5	A/µs
Regulator Output DC+AC Voltage Tolerance	Reg_DC_AC_Tol	-2.5		2.5	%
Regulator Feedback Setpoint Accuracy	FB_Set_Point	-0.75		0.75	%

Table 6: SWC Single Phase Regulator; DC+AC Specification

JEDEC Compliant Performance

DC-DC	Efficiency (% of Max I_{tdc} Load)			
	Light Load	25%	50%	100%
SWA, SWB	>83%	≥90 %	≥88 %	≥82 %
SWA + SWB	>83%	≥90 %	≥88 %	≥82 %
SWC	>85%	≥90 %	≥89 %	≥85 %

Table 7: Endura Technologies Implementation – Estimated Efficiency of DC-DC converters

Conditions:

- *V_{IN} = 5V*
- *Light Load: 100 mA SWA, SWB single-phase mode; 200 mA SWA+SWB dual-phase mode; 10mA SWC*
- *When efficiency of a given output regulator is measured, all other switching output regulators are disabled*
- *No external load on $V_{OUT\_1.8V}$, $V_{OUT\_1.0V}$ LDO is applied*
- *I2C/I3C bus is pulled High and held static. PWR_GOOD and GSI_n signals are pulled High and held static*
- *Efficiency includes Buck regulator loss, PCB loss (< 4 mΩ) and inductor loss. Inductor specification: SWA & SWB: L = 0.68uH, DCR_{Max} = 18.5 mΩ, ACR_{Max} @1MHz = 113 mΩ; SWC: L = 1.5uH, DCR_{Max} = 75 mΩ, ACR_{Max} @1MHz = 300 mΩ*
- *Efficiency calculation: (V_{OUT} * I_{OUT}) / (V_{IN} * I_{VIN}), where V_{OUT}, I_{OUT}, V_{IN}, I_{VIN} are measured values*
- *Maximum ambient temperature: 65°C (PMIC T_J 105°C); inductor characteristics at 105°C*
- *Output Buck regulator switching frequency can be set anywhere within 750kHz to 1000kHz*
- *Inductor value = 680nH for SWA and SWB output. The inductor value = 1.5uH for SWC output*

Summary & Conclusion

As computing platforms like DDR5, SSD and others grow in prominence, along with form factor and power dissipation challenges (Memory DIMM, Gen5 PCIe M.2 form factor, etc.), the need for companion power management solutions will be a key enabler.

This implementation of Endura Technologies' power delivery architecture is designed to fulfill these needs. Along with JEDEC PMIC5100 compliance, it will enable system design flexibility to select the ideal switching frequency to:

- Optimize efficiency across load currents
- Ramp faster and reduce warm-up times
- Minimize component count
- Reduce area footprints

Bibliography

Samsung. (2021, May 18). *Samsung Newsroom*. Retrieved from https://news.samsung.com/global/samsung-unveils-new-power-management-solutions-for-ddr5-modules

Wikipedia. (2022, July 05). *DDR5 SDRAM*. Retrieved from https://en.wikipedia.org/wiki/DDR5_SDRAM